FORM PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY DOCKET NO. 826.1903	APPLICATION NO. 10-705 847
LIST OF REFERENCES CITED BY APPLICANT *(Use several sheets if necessary)*		FIRST NAMED INVENTOR Hiroyuki HIGUCHI	
		FILING DATE November 13, 2003	GROUP ART UNIT

U.S. PATENT DOCUMENTS
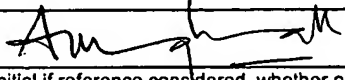
EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA						
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	AD						
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FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION YES	NO
	AG							
	AH							
	AI							
	AJ							
	AK							
	AL							

OTHER REFERENCES (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

N NJD	AM	H. HIGUCHI, "An Implication-based Method to Detect Multi-Cycle Paths in Large Sequential Circuits", In Proceedings of the 39th ACM/IEEE Design Automation Conference, pages 164-169.
NNJD	AN	K. NAKAMURA, et al., "Waiting False Path Analysis of Sequential Logic Circuits for Performance Optimization", IEEE/ACM ICCAD 98 pp. 392-395, 2002
NNJD	AO	S. DAVADAS et al., "Logic Synthesis", p. 236-241, McGraw-Hill, 1994

EXAMINER	DATE CONSIDERED 02/13/06

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.